COURSE OUTLINE

Course Code: CSE 305

Course Title: Computer Architecture

Level/Term: 3-I **Section:** A and B

Academic Session: July 2016

Course Teachers:

Name	Room No.	Email	Contact No.
Rifat Shahriyar (RS)	309	rifat1816@gmail.com	01777403791
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Syllabus:

Information representation; Measuring performance; Instructions and data access methods: operations and operands of computer hardware, representing instruction, addressing styles; Arithmetic Logic Unit (ALU) operations, floating point operations, designing ALU; Processor design: datapaths - single cycle and multicycle implementations; Control Unit design - hardwared and microprogrammed; Hazards; Exceptions; Pipeline: pipelined datapath and control, superscalar and dynamic pipelining; Memory organization: cache, virtual memory, channels; DMA and Interrupts; Buses; Multiprocessors: types of multiprocessors, performance, single bus multiprocessors, multiprocessors connected by network, clusters.

Learning Outcomes/Objectives:

After undergoing this course, students should be:

i. Able to grasp the basic concept of computer architecture and organization, and understand the key skills of constructing cost-effective computer systems.

ii. Able to evaluate different designs and organizations of modern computers to provide quantitative arguments in evaluating different designs.

iii. Able to articulate design issues in the design and development of different components of a computer such as processor, memory, and control unit etc.

iv. Able to understand the design issues of scalable and parallel computer architectures to cope up with future high performance computing systems.

Distribution of Marks:

Class participation	10%
Homework assignment and quizzes	20%
Final Examination (3 hours)	70%
Total	**100%**

Weekly Schedule:

Week	Topics	Teacher's Initial
1 + 2	Computer Abstractions and Technology	*RS*
3 + 4 + 5	Instructions: Language of the Compiler	*JMM*
5 + 6 + 7	Arithmetic for Computers	*JMM*
8 + 9	Parallel Processors from Client to Cloud	*JMM*
10 + 11 + 12	The Processor	*RS*
12 + 13 + 14	Large and Fast: Exploiting Memory Hierarchy	*RS*
14	Current Trends in Computer Architecture	*RS*

Prepared by:	
Name: **Rifat Shahriyar** Signature: Date:	Name: **Johra Muhammad Moosa** Signature: Date: